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-	71	((((((flip$1flop) or (flip adj flop)) and (net$1list or (net adj list))) and (((adjust$5 or chang$5 or modif$5) and (delay)) same (element))) and (hold)) and (hold same time)) and (skew)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/09/26 22:39
-	54	(((((((flip$1flop) or (flip adj flop)) and (net$1list or (net adj list))) and (((adjust$5 or chang$5 or modif$5) and (delay)) same (element))) and (hold)) and (hold same time)) and (skew)) and (frequenc$4)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/09/26 22:38
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1 Optimization: Performance optimization of single-phase level-sensitive circuits using time borrowing and non-zero clock skew
Baris Taskin, Ivan S. Kourtev
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**
Full text available: pdf(99.49 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a linear programming (LP) formulation for performance optimization of large-scale, synchronous circuits with level-sensitive latches. The proposed formulation permits circuits to operate at a higher clock frequency---that is, with a lower clock period---by the application of both non-zero clock skew scheduling [7] and time borrowing [9]. This LP formulation is computationally efficient and demonstrates significant circuit performance improvement. Unlike the approach document ...

Keywords: clock skew, cycle stealing, linear programming, optimization

2 Clock skew optimization for ground bounce control
Ashok Vittal, Hein Ha, Forrest Brewer, Malgorzata Marek-Sadowska
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(56.58 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

High speed synchronous digital systems require large switching currents to facilitate rapid signal transitions. These large currents create voltage drops on the power distribution network and necessitate expensive chip packaging with a large number of supply pins. In this paper we propose a novel technique to reduce the dynamic transient current drawn from the supply pins. Our approach is based on sub-dividing the synchronous clocking into multiple sub-clocks with relative skew. This spreads the ...

3 Concurrent flip-flop and repeater insertion for high performance integrated circuits
Pasquale Cocchini
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Additional Information: full citation, abstract, references, citings, index

Full text available: pdf(229.63 KB) terms

For many years, CMOS process scaling has allowed a steady increase in the operating frequency and integration density of integrated circuits. Only recently, however, have we reached a point where it takes several clock cycles for global signals to traverse a complex digital system such as a modern microprocessor. Thus, interconnect latency must be taken into account in current and future design tools at the architectural as well as synthesis level. To this purpose, this work proposes a new laten ...

4 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

5 Power efficient design for arithmetic circuits: Reducing pipeline energy demands with local DVS and dynamic retiming

Seokwoo Lee, Shidhartha Das, Toan Pham, Todd Austin, David Blaauw, Trevor Mudge

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(425.83 KB) Additional Information: full citation, abstract, references, index terms

The quadratic relationship between voltage and energy has made dynamic voltage scaling (DVS) one of the most powerful techniques to reduce system power demands. Recently, techniques such as Razor DVS, voltage overscaling, and Intelligent Energy Management have emerged as approaches to further reduce voltage by eliminating costly voltage margins inserted into traditional designs to ensure always-correct operation. The degree to which a global voltage controller can shave voltage margin ...

Keywords: dynamic retiming with global DVS, local DVS, razor

6 Power grid design and analysis techniques: Buffer sizing for clock power minimization subject to general skew constraints

Kai Wang, Malgorzata Marek-Sadowska

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(193.65 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we investigate the problem of buffer sizing for clock power minimization subject to general skew constraints. A novel approach based on sequential linear programming is presented. By taking the first-order Taylor's expansion of clock path delay

with respect to buffer widths, the original nonlinear problem is transformed to a sequence of linear programs, which incorporate clock skew scheduling and buffer sizing to minimize clock power dissipation. For each linear program, the sensi ...

Keywords: clock skew scheduling, sequential linear programming, sizing

7 Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation

Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Rajeev Rao, Toan Pham, Conrad Ziesler, David Blaauw, Todd Austin, Krisztian Flautner, Trevor Mudge

December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture**

Full text available: pdf(568.17 KB) Publisher Site

Additional Information: full citation, abstract, citings, index terms

With increasing clock frequencies and silicon integration,power aware computing has become a critical concernin the design of embedded processors and systems-on-chip.One of the more effective and widely used methods for power-awarecomputing is dynamic voltage scaling (DVS). In orderto obtain the maximum power savings from DVS, it is essentialto scale the supply voltage as low as possible while ensuringcorrect operation of the processor. The critical voltage ischosen such that under a worst-case ...

8 UST/DME: a clock tree router for general skew constraints

Chung-wen Albert Tsao, Cheng-kok Koh

July 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 3

Full text available: pdf(260.87 KB)

Additional Information: full citation, abstract, references, citings, index terms

In this article, we propose new approaches for solving the useful-skew tree (UST) routing problem [Xi and Dai 1997]: clock routing subject to general skew constraints. The clock layout synthesis engine of our UST algorithms is based on the deferred-merge embedding (DME) paradigm for the zero-skew tree (ZST) [Edahiro 1992; Chao et al. 1992] and bounded-skew tree (BST) [Cong and Koh 1995; Huang et al. 1995; Kahng and Tsao 1997; Cong et al. 1998] routings; hence, the names UST/DME and Greedy-UST/DM ...

Keywords: Useful Skew, clock tree, feasible skew range, incremental skew scheduling, merging and embedding, merging region

9 Interconnect pipelining in a throughput-intensive FPGA architecture

Amit Singh, Arindam Mukherjee, Malgorzata Marek-Sadowska

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(203.52 KB)

Additional Information: full citation, abstract, references, citings, index terms

Wave-steering is a new design methodology that realizes high throughput circuits by embedding layout friendly synthesized structures in silicon. In the wave-steering design methodology, cirðcuits inherently utilize latches. Inside the synthesized structures they are used for signal skewing, and on the interconnects to guarðantee the correct arrival times at the inputs. Recently, we proposed a novel high-throughput FPGA architecture based on the wave-steering design principle to handle throu ...

10 Architecture issues and solutions for a high-capacity FPGA

Steve Trimberger, Khue Duong, Bob Conn

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-**

programmable gate arrays

Full text available: pdf(756.17 KB) Additional Information: full citation, references, citings, index terms

11 Design strategies for active power reduction: A 225 MHz resonant clocked ASIC chip

Conrad H. Ziesler, Joohee Kim, Visvesh S. Sathe, Marios C. Papaefthymiou

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(262.51 KB) Additional Information: full citation, abstract, references, index terms

We have recently designed, fabricated, and successfully tested an experimental chip that validates a novel method for reducing clock dissipation through energy recovery. Our approach includes a single-phase sinusoidal clock signal, an L-C resonant sinusoidal clock generator, and an energy recovering flip-flop. Our chip comprises a dual-mode ASIC with two independent clock systems, one conventional and one energy recovering, and was fabricated in a micron bulk CMOS process. The ASIC computes a pi ...

Keywords: CMOS, VLSI, adiabatic logic, clock generator, flip-flop, low energy, resonant LC tank, single phase

12 A unified algorithm for gate sizing and clock skew optimization to minimize sequential circuit area

Weitong Chuang, Sachin S. Sapatnekar, Ibrahim N. Hajj

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(462.52 KB) Additional Information: full citation, references, citings

13 A novel high throughput reconfigurable FPGA architecture

Amit Singh, Luca Macchiarulo, Arindam Mukherjee, Malgorzata Marek-Sadowska

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

Full text available: pdf(714.12 KB) Additional Information: full citation, abstract, references, citings, index terms

With increased logic density due to the shift towards Deep Submicron technologies (DSM), FPGAs have become a viable option for implementing large designs. However, most commercial FPGAs, due to their general purpose architectural nature, cannot handle designs which require very high throughput. In this paper, we propose a novel high throughput FPGA architecture which tries to combine the high-performance of Application Specific Integrated Circuits (ASICs) and the flexibility afforded by the ...

14 Reconfigurable computing: a survey of systems and software

Katherine Compton, Scott Hauck

June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2

Full text available: pdf(710.56 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single chip architectures to multi-chip systems, including internal structures and external coupling. W ...

Keywords: Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, reconfigurable computing, reconfigurable systems

15 TIM: a timing package for two-phase, level-clocked circuitry
Marios C. Papaefthymiou, Keith H. Randall
July 1993 **Proceedings of the 30th international conference on Design automation**
Full text available: pdf(700.40 KB) Additional Information: full citation, references, citings, index terms

16 An innovative, segmented high performance FPGA family with variable-grain-architecture and wide-gating functions
Om Agrawal, Herman Chang, Brad Sharpe-Geisler, Nick Schmitz, Bai Nguyen, Jack Wong, Giap Tran, Fabiano Fontana, Bill Harding
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**
Full text available: pdf(2.87 MB) Additional Information: full citation, references, citings, index terms

17 Parallel logic simulation of VLSI systems
Mary L. Bailey, Jack V. Briner, Roger D. Chamberlain
September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3
Full text available: pdf(3.74 MB) Additional Information: full citation, abstract, references, citings, index terms

Fast, efficient logic simulators are an essential tool in modern VLSI system design. Logic simulation is used extensively for design verification prior to fabrication, and as VLSI systems grow in size, the execution time required by simulation is becoming more and more significant. Faster logic simulators will have an appreciable economic impact, speeding time to market while ensuring more thorough system design testing. One approach to this problem is to utilize parallel processing, taking ...

Keywords: circuit structure, parallel architecture, parallelism, partitioning, synchronization algorithm, timing granularity

18 The associative-skew clock routing problem
Yu Chen, Andrew B. Kahng, Gang Qu, Alexander Zelikovsky
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(109.97 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce the associative skew clock routing problem, which seeks a clock routing tree such that zero skew is preserved only within identified groups of sinks. The associative skew problem is easier to address within current EDA frameworks than useful-skew (skew-scheduling) approaches, and defines an interesting tradeoff between the traditional zero-skew clock routing problem (one sink group) and the Steiner minimum tree problem (n sink ...

19 Computing optimal clock schedules
T. G. Szymanski
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(630.15 KB) Additional Information: full citation, references, citings, index terms

20 Placement for clock period minimization with multiple wave propagation

Donald A. Joy, Maciej J. Ciesielski

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

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1 Optimization: Performance optimization of single-phase level-sensitive circuits using time borrowing and non-zero clock skew

Baris Taskin, Ivan S. Kourtev

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Keywords: clock skew scheduling, sequential linear programming, sizing

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November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

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Full text available: pdf(700.40 KB) Additional Information: full citation, references, citings, index terms

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Keywords: circuit structure, parallel architecture, parallelism, partitioning, synchronization algorithm, timing granularity

8 Computing optimal clock schedules

T. G. Szymanski

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(630.15 KB) Additional Information: full citation, references, citings, index terms

9 Self-assessment procedure XVI: a self-assessment procedure dealing with computer organization and logic design

Glen G. Langdon

November 1986 **Communications of the ACM**, Volume 29 Issue 11

Full text available: pdf(908.13 KB) Additional Information: full citation, abstract, references, index terms

A self-assessment procedure dealing with computer organization and logic design

10 Interface timing verification drives system design

Ajay J. Daga, Peter R. Suaris

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(144.39 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

System design, i.e. the design of board-level circuits andsystems-on-a-chip, focuses on the integration of off-the-shelf andapplication-specific VLSI components. A key aspect of systemdesign is to ensure the satisfaction of component interface timingrequirements. This is necessary for the correct exchange ofinformation among components on a system. We present amethodology for the interface timing verification and subsequenttiming-driven floorplanning of systems. We present results on theapplicat ...

11 Minimum padding to satisfy short path constraints

Narendra V. Shenoy, Robert K. Brayton, Alberto L. Sangiovanni-Vincentelli

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(561.10 KB) Additional Information: full citation, references, citings

12 Lazy transition systems: application to timing optimization of asynchronous circuits

Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, Alexander Taubin, Alex Yakovlev

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

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Speek, H.; Kerkhoff, H.G.; Sachdev, M.; Shashaani, M.;
European Test Workshop, 2000. Proceedings. IEEE , 23-26 May 2000
Pages:3 - 8

[Abstract] [PDF Full-Text (468 KB)] **IEEE CNF**

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Maymandi-Nejad, M.; Sachdev, M.;
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11 **Restructuring for fault-tolerant systolic arrays**
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